

With regard to ground (i), Applicant initially notes that the output indicator in the claims at issue is not a structural element of such claims, and is instead a signal generated by the output load detection circuit. Thus, a structural relationship between this non-structural claim element and the current generator circuit, the input stage or the output stage need not be recited in the claims at issue in order for such claims to comply with §112.

Also, the claims at issue in fact do make clear the structural relationship between the current generator circuit, the input stage and the output stage. For example, claim 1 explicitly calls for “the output stage being operatively coupled to the input stage,” and further specifies that the current generator circuit is “adapted to establish a modulation current for application to one of a first output and a second output of the output stage in accordance with an input data signal applied to the input stage.” Thus, claim 1 recites specific structure relationships between the current generator circuit, the input stage and the output stage.

With regard to ground (ii), the claims at issue explicitly recite that the output load detection circuit is “configured to detect an improper load condition at one or more of the first and second outputs of the output stage.” Given this explicit recitation, it is difficult to imagine how the Examiner could argue that it is somehow unclear what the output load detection circuit is used to detect.

The specification at page 5, line 22 to page 9, line 28 describes, in conjunction with FIGS. 3, 4 and 5 of the drawings, an illustrative embodiment of a driver circuit meeting the above-noted limitations of claims 1, 16 and 17. The Examiner is invited to review the cited portions of the application in order to obtain a better understanding regarding the various elements recited in these claims.

In view of the above, the §112 rejection is believed to be without merit, and should be withdrawn.

Claims 1, 2, 5, 10, 11 and 13-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,560,256 (hereinafter “Seki”). Applicant respectfully traverses the §102(e) rejection, for the reasons specified below.

Applicant initially notes that the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated “only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference,” citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the “identical invention . . . in as complete detail as is contained in the . . . claim,” citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicant respectfully submits that the Examiner has failed to establish anticipation of at least independent claims 1, 16 and 17 by the Seki reference.

Each of independent claims 1, 16 and 17 calls for a driver circuit which includes an output load detection circuit having first and second inputs coupled to respective first and second outputs of an output stage of the driver circuit. The output load detection circuit is configured to detect an improper load condition at one or more of the first and second outputs of the output stage of the driver circuit and to generate a corresponding output indicator. The output indicator is utilizable in the driver circuit to control the modulation current so as to prevent saturation of at least one device in the output stage in the presence of the improper load condition.

Advantageously, the invention as claimed can prevent undesirable saturation of the output stage of a driver circuit under fault conditions, such as failure to connect a laser diode or other optical source to the driver circuit output prior to operation of the driver circuit, while also maintaining the ability of the driver circuit to operate at high speeds. See the specification at, for example, page 1, line 26 to page 2, line 16 and page 3, lines 9-11.

Applicant submits that the Seki reference fails to teach or suggest at least the above-noted limitations of each of independent claims 1, 16 and 17, and furthermore fails to provide the associated advantages of the claimed invention.

The Examiner in formulating the §102(e) rejection argues that Seki in FIG. 1 thereof shows a driver circuit meeting the above-noted limitations of independent claims 1, 16 and 17. However, the laser driver circuit in FIG. 1 of Seki does not include an output load detection circuit configured in the manner claimed.

More specifically, FIG. 1 of Seki fails to show an output load detection circuit having first and second inputs coupled to respective first and second outputs of an output stage of a driver circuit. In addition, there is no element in FIG. 1 of Seki that is configured to detect an improper load condition at one or more of the first and second outputs of the output stage of the driver circuit. Moreover, there is no element in FIG. 1 of Seki that generates an output indicator utilizable in the driver circuit to control modulation current so as to prevent saturation of at least one device in the output stage of the driver circuit in the presence of the improper load condition.

Instead, FIG. 1 of Seki includes a photodiode (PD) 1c “for monitoring amounts of light from LD1 and LD2” which correspond to respective laser diodes 1a and 1b (Seki, column 3, lines 17-20). The PD 1c is part of a feedback control loop which simply detects and controls the optical output of laser diodes LD1 (1a) and LD2 (1b). As noted above, this does not teach or suggest the claimed output load detection circuit, configured to detect an improper load condition at one or more of the first and second outputs of an output stage of the driver circuit, and operative to generate an output indicator utilizable in the manner claimed.

The present invention, in contrast to the arrangement in FIG. 1 of Seki, configures a driver circuit to include an output load detection circuit which can detect, among other improper load conditions, the failure to connect a laser diode or other optical source to the driver circuit prior to operating the driver circuit. The claimed arrangement advantageously protects the driver circuit itself under such conditions, by preventing the saturation of at least one device in the output stage thereof. The Seki arrangement does not provide this advantage of the claimed arrangements, and similarly fails to provide the other advantages noted previously herein.

Accordingly, it is respectfully submitted that Seki fails to teach or suggest the limitations of each of independent claims 1, 16 and 17. The §102(e) rejection is believed to be improper and should be withdrawn.


Claims 3, 4 and 6-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Seki in view of U.S. Patent No. 5,883,910 (hereinafter “Link”). Applicant respectfully traverses the §103(a) rejection. The Link reference fails to supplement the above-described deficiencies of the Seki reference as applied to the corresponding independent claim 1. Claims 3, 4 and 6-8 are

therefore believed allowable for at least the reasons identified above with regard to independent claim 1.

Claims 9 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Seki in view of U.S. Patent No. 6,266,078 (hereinafter "Koga"). Applicant respectfully traverses the §103(a) rejection. The Koga reference fails to supplement the above-described deficiencies of the Seki reference as applied to the corresponding independent claim 1. Claims 9 and 12 are therefore believed allowable for at least the reasons identified above with regard to independent claim 1.

In view of the above, Applicant believes that claims 1-17 are in condition for allowance, and respectfully requests withdrawal of the §112, §102(e) and §103(a) rejections.

Respectfully submitted,

A handwritten signature in black ink that reads "Joseph B. Ryan". The signature is written in a cursive, flowing style with a large, prominent "J" and "R".

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